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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,845	08/26/2005	Martin Vorbach	2885/86	9148

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EXAMINER	
VICARY, KEITH E	

ART UNIT	PAPER NUMBER
2183	

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08/07/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/501,845	VORBACH ET AL.	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-13,15-17 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13,15-17 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/20/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

0. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/20/2009 has been entered.

1. Claims 7-13, 15-17, and 19-22 are pending in this examination and presented for examination. Claims 7, 19, and 21-22 are currently amended by an amendment filed 7/20/2009.

Claim Objections

2. Claim 10 is objected to because of the following informalities. Appropriate correction is required.

a. Claim 10 recites the limitation "PAE." It is indefinite as to what this limitation stands for; the acronym should be expanded

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 10 recites the limitation "the register is a RAM PAE" in lines 1-2. It is indefinite as to how a register can be a RAM.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7, 10-11,15-17, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (Smith) (US 6658564 B1) in view of Dockser (US 5860119) in view of Borkenhagen et al. (Borkenhagen) (US 6076157).

8. Consider claim 7, Smith discloses providing a program corresponding to a sequence of compilable high-level language instructions (col. 10, lines 49-50, high-level design specification or algorithm); determining, for the reconfigurable field of data processing cells (col. 8, lines 52-53, programmable logic resources), a set of configurations by execution of which the program is run (col. 11, lines 60-63, compiling hardware functions into configuration patterns using a hardware description language

compiler); executing the configurations (col. 10, lines 50-51, executing on a reconfigurable hardware architecture); and during the executing: storing, in the data stream memory, at least one of the data stream and parts of the data stream (col. 4, lines 22-33, disclose of the random-access memory devices, it is inherent may be written to, the data with which it is written constitutes all or part of a data stream), wherein the data stream memory stores at least one vector (it is inherent that a data stream memory holds vectors of bits, such as each addressable line).

However, Smith does not explicitly disclose that the data stream memory is a register which is operated as a FIFO memory. Smith also does not disclose determining, for each configuration, a respective maximum allowed execution runtime prior to lapse of which the respective configuration is uninterruptible, and for each configuration, monitoring the respective maximum allowed execution runtime in order to interrupt the configuration if the respective maximum allowed execution runtime is exceeded.

On the other hand, Dockser does disclose a register which is operated as a FIFO memory to process a data stream (e.g. col. 12, line 16-17, FIFO registers).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that one of many motivations of having a register act as a memory would be to allow quick access to data, and a FIFO buffer preserves order of incoming data (Dockser, col. 1, lines 63-65). In addition, Dockser makes a FIFO system both simple and inexpensive to implement (Dockser, col. 4, lines 6-40), despite decreases in management overhead.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Dockser with the invention of Smith in order to allow quicker access to the data stream while preserving order of incoming data in a simple and inexpensive manner.

However, neither Smith nor Dockser disclose determining, for each configuration, a respective maximum allowed execution runtime prior to lapse of which the respective configuration is uninterruptible, and for each configuration, monitoring the respective maximum allowed execution runtime in order to interrupt the configuration if the respective maximum allowed execution runtime is exceeded. However, note that Smith discloses of a threads as configurations, and wherein switching threads involves reconfiguring a reconfigurable unit to the configuration (col. 2, line 25-29, which discloses of threads correlating to software functions and configurations correlating to hardware functions; col. 1, line 55, discloses of the reconfigurable logic aspect).

On the other hand, Borkenhagen does disclose of determining, for each thread, a respective maximum allowed execution runtime prior to lapse of which a respective thread is uninterruptible, and for each thread, monitoring the respective maximum allowed execution runtime in order to interrupt the thread if the respective maximum allowed execution runtime is exceeded (col. 15, lines 1-19, thread switch time-out values forces a thread switch; col. 14, lines 65-67, each thread need not have the same thread switch time-out value).

Borkenhagen's teaching prevents processor hangs (Borkenhagen, col. 5, lines 35-37).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Borkenhagen with the invention of Smith and Dockser in order to prevent processor hangs.

9. Consider claim 10, Smith discloses that the register is a RAM PAE (col. 4, lines 22-33, disclose of the random-access memory devices).

10. Consider claim 11, the combination of Smith, Dockser, and Borkenhagen discloses using the register to provide read and write access (Borkenhagen, col. 4, lines 32-35, receive mode and transmit mode, and col. 5, lines 56-65, read and write pointers) when a virtual FIFO dividing line is implemented (Borkenhagen, col. 3, lines 10-30, lines 54-56; the last word flag and end-of-packet detection means correlate to the said virtual FIFO dividing line), wherein the program includes a multitask application, and a register is used for execution of at least one of two different tasks of the multitask application (Smith and Borkenhagen discloses of multithreading; alternatively, multiple tasks within a thread).

11. Consider claim 15, Borkenhagen discloses a watchdog is used to recognize an exceedance of each respective maximum allowed execution runtime (col. 15, lines 1-19, thread switch time-out values from the thread switch time0out register forces a thread switch).

12. Consider claim 16, Borkenhagen discloses that any one of the configurations that exceeds its respective maximum allowed execution runtime is treated as illegal (col. 15, lines 1-19, thread switch time-out values forces a thread switch).

13. Consider claim 17, Borkenhagen discloses that any one of the configurations that exceeds its respective maximum allowed execution runtime is treated as illegal (col. 15, lines 1-19, thread switch time-out values forces a thread switch).

14. Consider claim 19, Smith and Borkenhagen discloses an operating system performs a predefined step in response to an exceedance by a configuration of the configuration's maximum allowed execution (Borkenhagen, col. 15, lines 1-19, thread switch time-out values forces a thread switch; col. 17, lines 41-42, operating system; Smith discloses in col. 8, lines 26-27, 52-53, discloses of operating systems allocating programmable logic resources to functions).

15. Consider claim 20, Smith discloses at least one of the configurations calls another of the configurations as a sub-routine (col. 12, lines 1-5 for example, a main function calls a dynamically-linked function).

16. Consider claim 21, Borkenhagen discloses the watchdog signal initiates a system trap (col. 15, lines 1-19, thread switch time-out values forces a thread switch; the time-out interrupts the currently running thread).

17. Consider claim 22, Smith and Borkenhagen discloses, in response to the system trap, an operating system performs steps defined for a response to an invalid instruction (Borkenhagen, col. 15, lines 1-19, thread switch time-out values forces a thread switch; col. 17, lines 41-42, operating system; Smith discloses in col. 8, lines 26-27, 52-53, discloses of operating systems allocating programmable logic resources to functions).

18. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, Dockser, and Borkenhagen as applied to claim 7 above, and further in view of Panwar et al. (Panwar) (US 5941977).

19. Consider claim 8, Smith, Dockser, and Borkenhagen do not disclose at least one: I) of a register allocation device to allocate the register, and ii) a register releasing device to release the register.

On the other hand, Panwar does disclose at least one: I) of a register allocation device to allocate the register, and ii) a register releasing device to release the register (col. 7, lines 31-39, register window allocation and col. 7, lines 54-64, register management).

Panwar's teaching enables processes to access registers independent of other processes executing within the processor (Panwar, col. 7, lines 35-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Panwar with the invention of Smith,

Dockser, and Borkenhagen in order to access registers independent of other processes executing within the processor.

20. Consider claim 9, Panwar discloses that the register allocation device is preserved over multiple reconfigurations of the reconfigurable field of data processing cells (col. 2, lines 25-42, col. 6, lines 32-36, col. 7, lines 31-39 and 54-64; the multithreading aspect in which each thread has its corresponding registers conserved correlates to the different reconfigurations as per Smith's correlation between configurations and threads as explained above).

21. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, Dockser, and Borkenhagen as applied to claim 7 above, and further in view of Davis et al. (Davis) (US PAT 4041462).

22. Consider claim 12, Smith, Dockser, and Borkenhagen do not explicitly disclose at least one memory unit configured for use as a stack and being configured to indicate at least one of a stack underflow state and a stack overflow state.

On the other hand, Davis does disclose at least one memory unit configured for use as a stack and being configured to indicate at least one of a stack underflow state and a stack overflow state (col. 14, lines 1-4, limit checking facilities which test for overflow and underflow, and lines 21-32, PSW)

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that stacks in general are an easily implemented method of dynamic

allocation of storage space for data, and a simple efficient mechanism for enqueuing data and/or parameters.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the stacks of Davis with the invention of Smith, Dockser, and Borkenhagen in order to easily implement a method of dynamic allocation of storage space for data, and efficiently enqueue data and/or parameters.

23. Consider claim 13, the claim is rejected for the same reasons as claim 12 above. In addition, Davis discloses the at least one of the underflow state and overflow state is of an operating system unit (col. 14, lines 1-4 and lines 21-32; also, note the PSW is typically accessed by the operating system).

Response to Arguments

24. Applicant argues in the paragraph spanning pages 6 and 7 that claim 7 has been clarified to indicate that the data stream memory is one operated as a FIFO memory, as opposed to Smith's random-access memory devices. In view of this, and to further prosecution, the above rejection uses Dockser to teach this newly added limitation. However, examiner notes that the limitation's location in the preamble may prevent it from being given patentable weight

25. Applicant argues on page 7 that Gee merely provides for a maximum allotted time for a set of instructions, but does not disclose a maximum allotted time for a

configuration. Applicant then makes various arguments regarding how a configuration does not correlate to a set of instructions; these are addressed in sequence below.

26. Applicant argues that "[a] configuration is of a function and/or interconnection of units for their use to execute instructions." Examiner first notes that this definition does not appear to be present in the instant disclosure or the instant claims. While this recitation is indefinite as it could mean multiple different things, examiner will subsequently read a configuration to be data which is used instead of an instruction in order to perform an operation. This interpretation is supported by both the instant application (page 7, "the traditional instruction is replaced by a configuration") and the Smith reference (e.g. col. 2, lines 4-8, which disclose that when an application is compiled, the functions of the application are partitioned into blocks of configuration data).

27. Given that applicant then argues that "[w]ith the setting of a maximum allotted time for an instruction or instruction set to which a configuration corresponds, the cited art does not suggest that there should also be set a maximum allotted time for the corresponding configuration. However, when a configuration directly correlates to some set of one or more instructions as it does in Smith, a maximum allotted time for that set of one or more instructions is necessarily also the maximum allotted time for the corresponding configuration.

28. Applicant argues that the cited art does not suggest contemplation of any need or benefit to such an additional or substitute maximum allotted time. However, as explained above, the examiner's combination does not entail any additional or substitute maximum allotted time. Rather, Smith teaches of replacing a set of one or more instructions with a configuration, and Gee teaches that a set of one or more instructions is assigned a maximum allotted time. The combination entails Smith's set of one or more instructions having a maximum alloted time. By definition, this maximum allotted time for the set of one or more instructions is necessarily the maximum allotted time for the configuration as well.

29. Applicant argues that the slices of Gee are not comparable to configurations. However, as noted above, a configuration corresponds to a set of one or more instructions. Moreover, Gee discloses in col. 3, line 54 that a slice is a partition. Gee discloses in col. 3, lines 44-45 that the partitions are of an application. Given that an application is comprised of program instructions, Gee's slices are thus comparable to a set of one or more instructions, and, as explained above, are thus also comparable to a configuration in the combination of Smith and Gee. In other words, Gee teaches of the desirability to prevent a set of one or more instructions from taking up too much time and keeping other instructions from running. This teaching is still clearly applicable regardless of whether the instructions are executed normally as software on a general-purpose microprocessor, or as configurations in a reconfigurable processor.

30. Applicant argues that configurations are for execution of instructions, so that the suggestion of a maximum allotted time for instructions would not further suggest a maximum allotted time to configurations which are for and correspond to those same instructions to which the maximum allotted time is already suggested to be set. However, in the environment wherein a configuration corresponds to a set of one or more instructions, a maximum allotted time for that set of one or more instruction necessarily is the same as a maximum allotted time for that configuration as well. In other words, the examiner is not arguing that an additional maximum allotted time for configurations is present in addition to the maximum allotted time for the instructions, but rather they are the same maximum allotted time.

31. Applicant argues that use of allotted maximum time to a configuration, in addition to or instead of one for the corresponding instructions, has not been contemplated by the prior art. However, examiner is not arguing that the allotted maximum time to corresponding instructions is being supplemented by allotted maximum time for the corresponding configuration, nor is examiner arguing that the allotted maximum time to corresponding instructions is being replaced by some other value which is representative of the allotted maximum time to corresponding configuration. Rather, the maximum allotted time for a set of one or more instructions also necessarily indicates the maximum allotted time for a configuration which corresponds to that set of one or more instructions.

32. Applicant argues on the paragraph spanning page 7 and 8 that the present application resolves a conflict which arises by it being highly preferable, on the one hand, to have configurations that run as long as possible due to lower configuration overhead, whereas, on the other hand, it is preferred to have a fast interrupt response time. However, these same considerations are analogous to Gee's considerations in implementing the watchdog timer for sets of instructions of the partition slices, and modifying these instructions to be configurations so that they can be implemented in reconfigurable hardware for performance reasons does not undermine the viability and motivation of Gee's teaching.

33. Applicant argues that the present application discusses how to handle loops if a maximum time is allotted to a configuration. However, there does not appear to be any limitations claimed regarding how to handle loops if a maximum time is allotted to a configuration.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

b. Paul et al. (US 20090085603) discloses of using a hardware watchdog timer for FPGA configurations.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 7:00 a.m. - 5:30 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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